Analog Front End for the fiber tracker in Dzero

I can tell you about the Dzero electronics, but I do not know what you want and/or need.

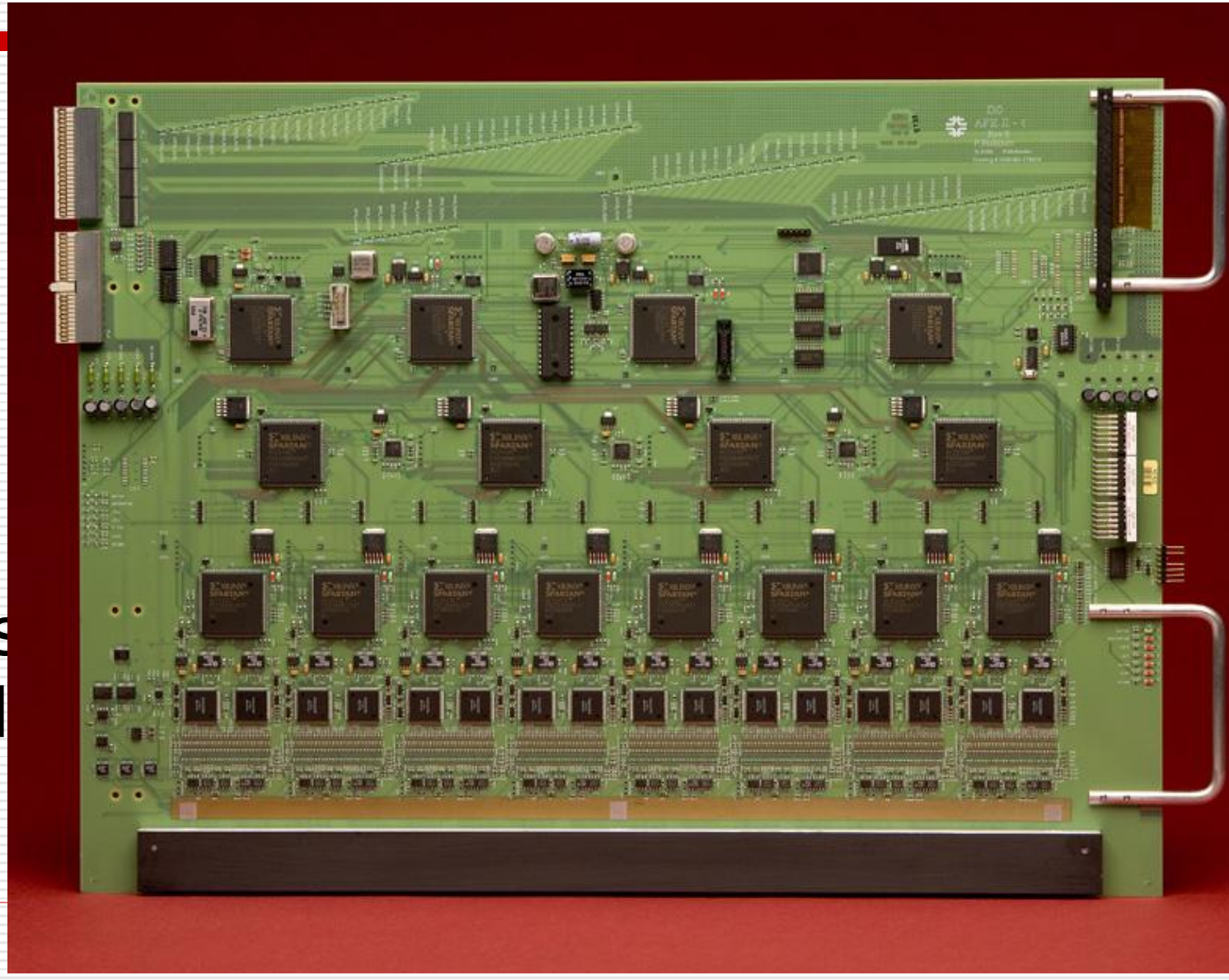
THIS IS NOT A LECTURE

LETS TALK

AFEII-t

Outline

- What
- How
- Why
- Lessons learned

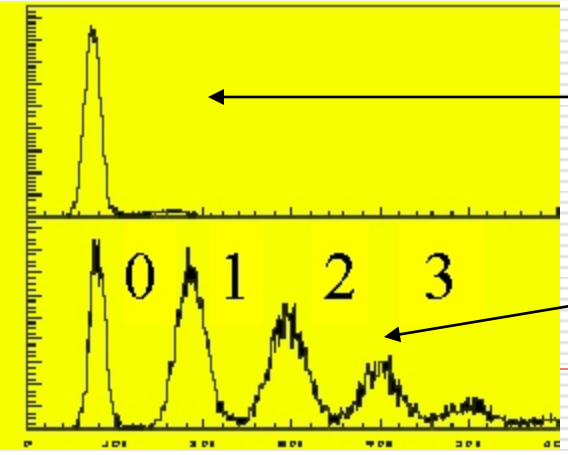


VLPC

Visible**L**ight**P**hoton**C**ounter

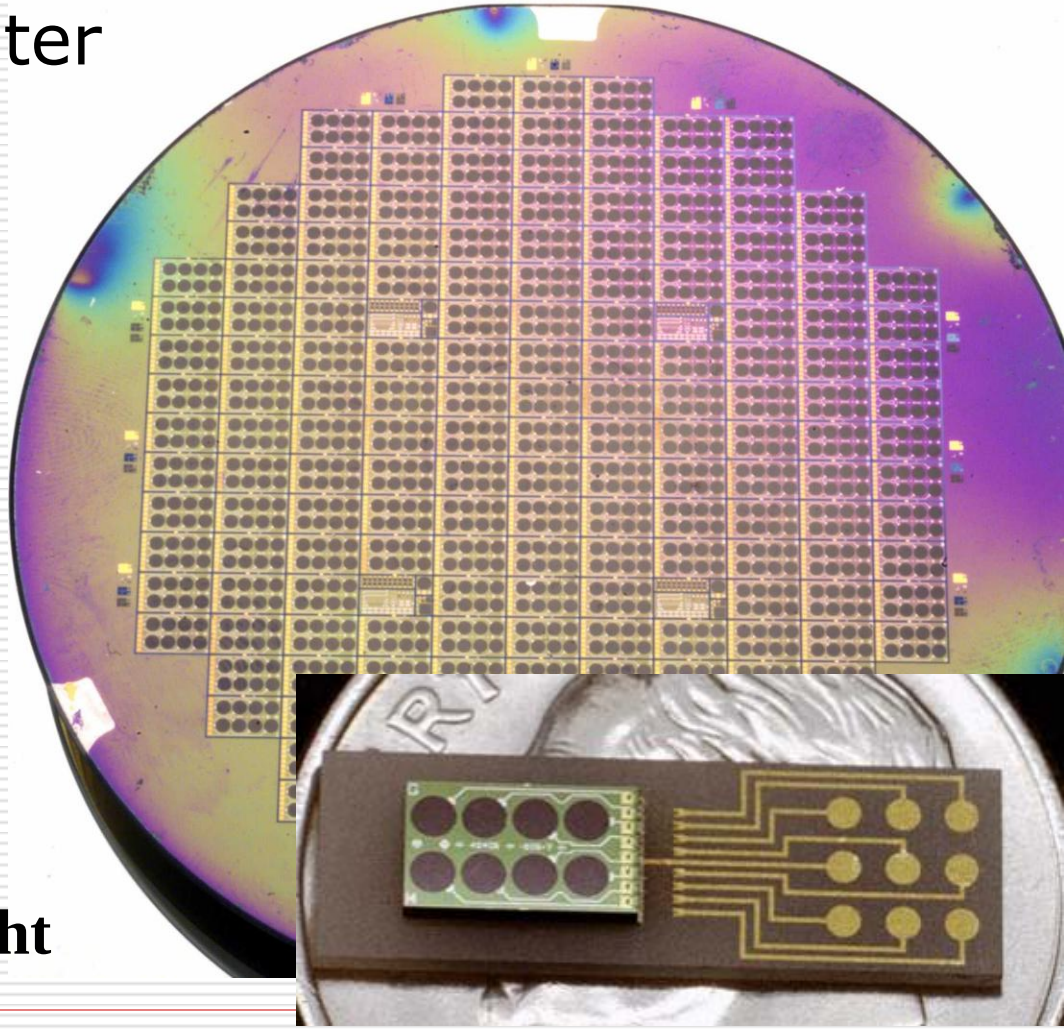
- very high QE
- good gain
- low noise

makes fiber tracker possible!

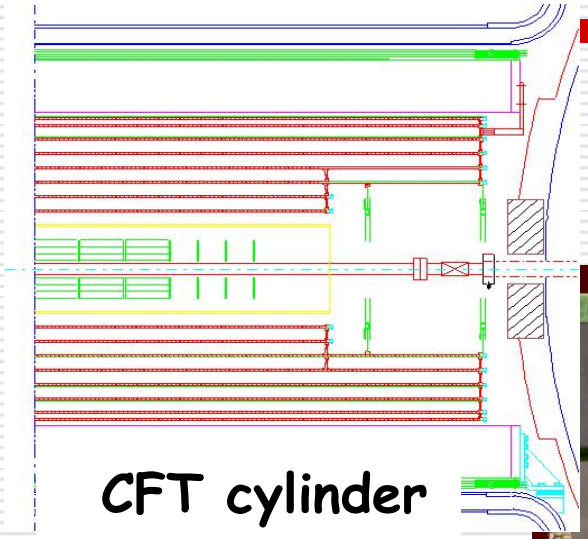


no light

a little light

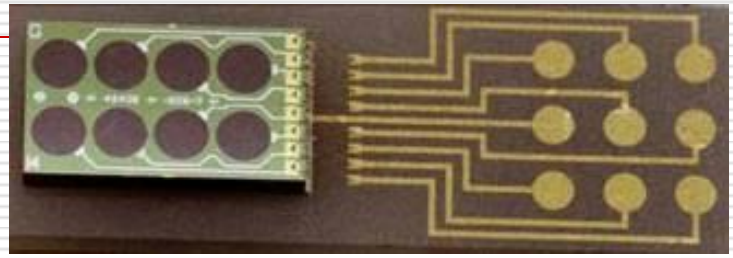


Analog Front End (AFE)



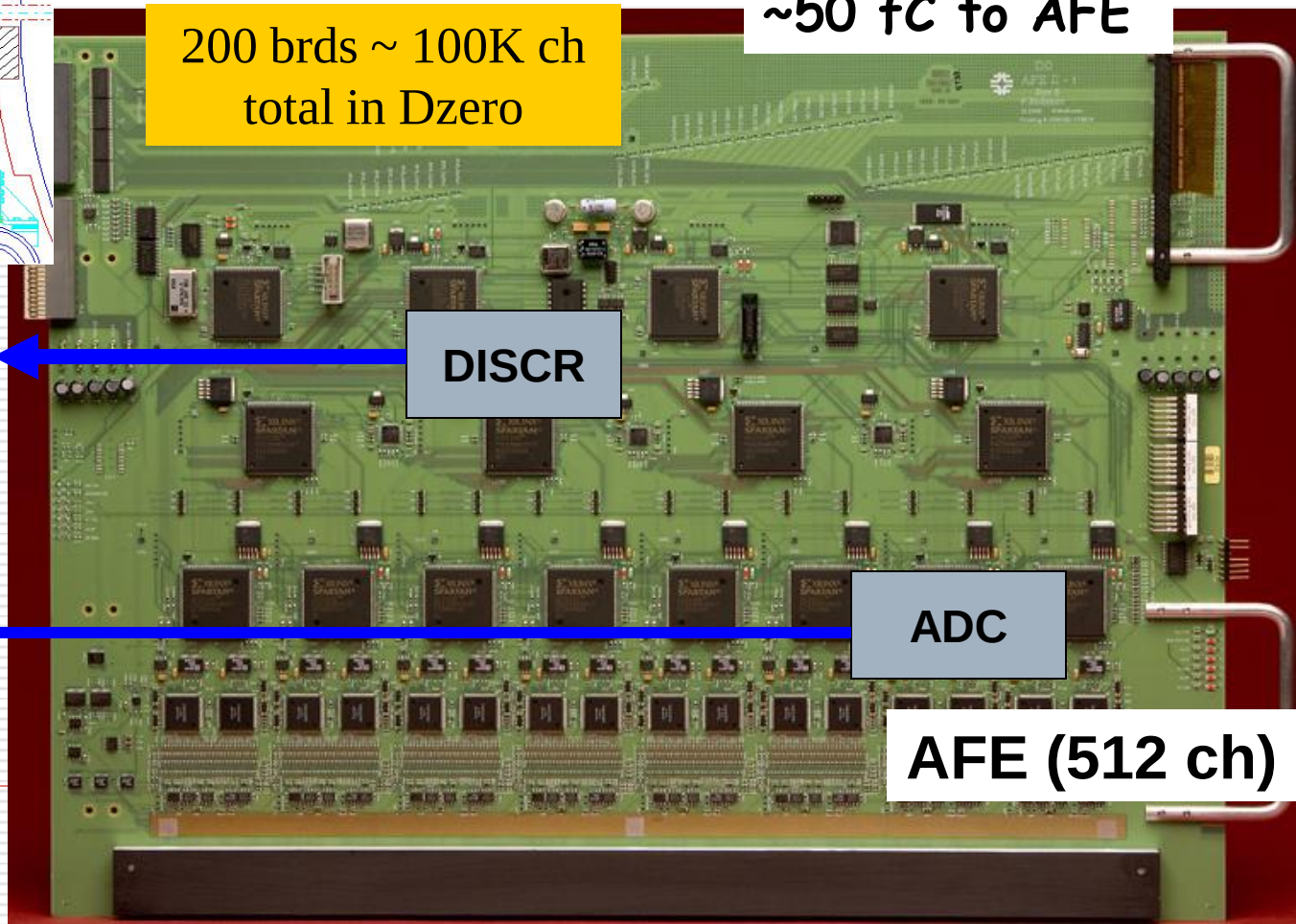
~8 photons from fiber

VLPC



~50 fC to AFE

200 brds ~ 100K ch total in Dzero



Discriminator output every 396 nsec for L1

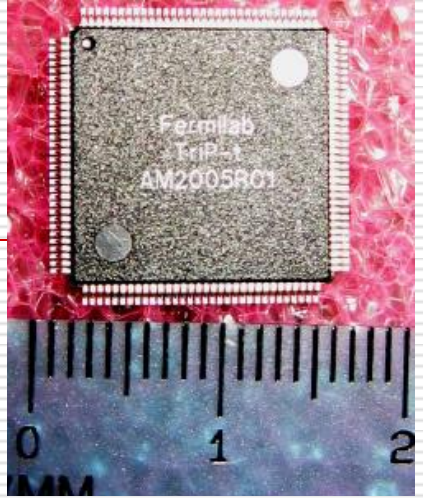
Amplitude signal readout for L3 and offline

Analog Front End (AFE)

3 main responsibilities

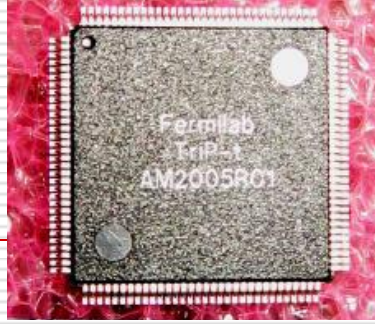
1. Care and feeding of the VLPCs (via slow control)
   - Bias (±40mV)
   - Temperature control (±0.05K)
2. Hit/no hit decision to the trigger system every crossing, every fiber.
   - Used in forming Level 1 decision
   - 512 ch/board, every BX (max 485 MB/s)
3. Amplify VLPC signals, digitize to 8 bits, zero suppress and readout every on L1 accept
   - max 40 MB/s
   - Readout via same system as silicon strip vertex detector

TriP-t

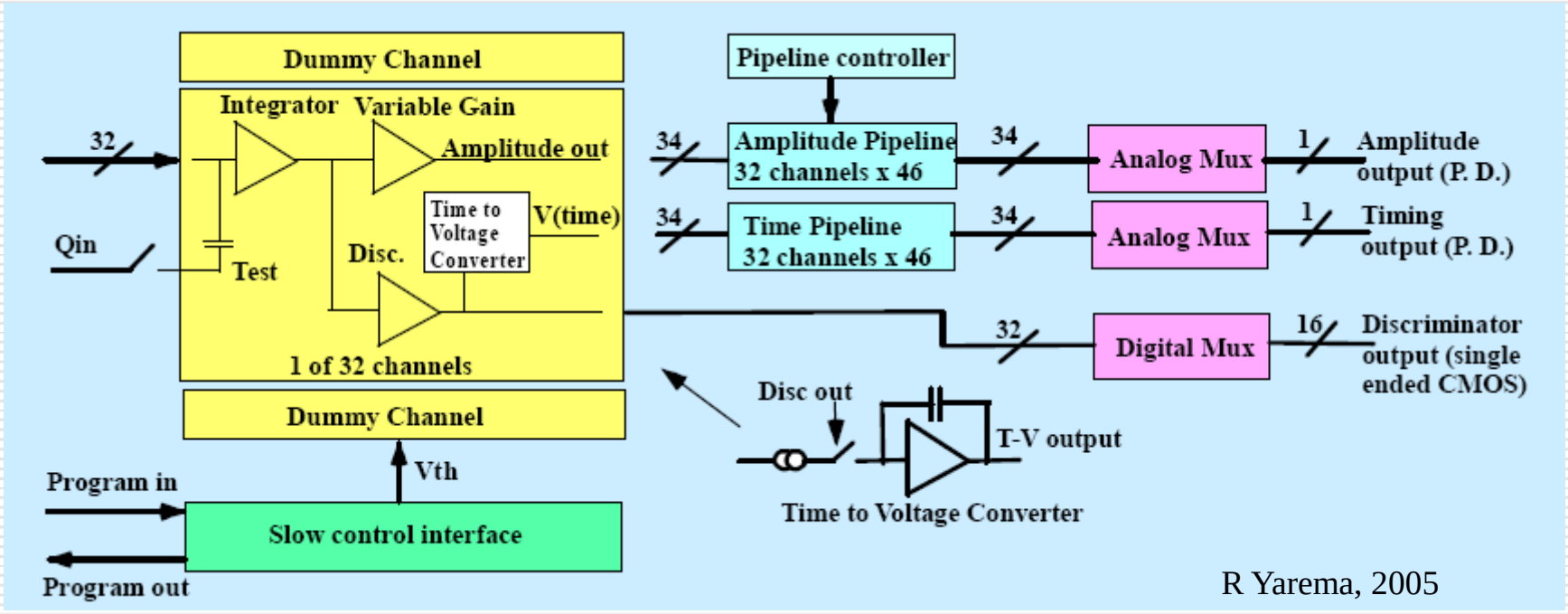


- AFE is designed around the TriP-t
  - Trigger and Pipeline – with timing
  - 32ch/chip: discr,48 cell analog pipeline ea.
  - 0.25um CMOS manufactured by TSMC
- TriP-t ASIC designed specifically for Dzero VLPC based detectors: CFT, CPS, FPS
- TriP-t designed by Fermilab ASIC group, A. Mekkaoui lead designer
- Fermilab has a strong ASIC group, lots of experience, wide range of capabilities
  - slow control from FPIX, pipeline from SVX4

TriP-t Block Diagram

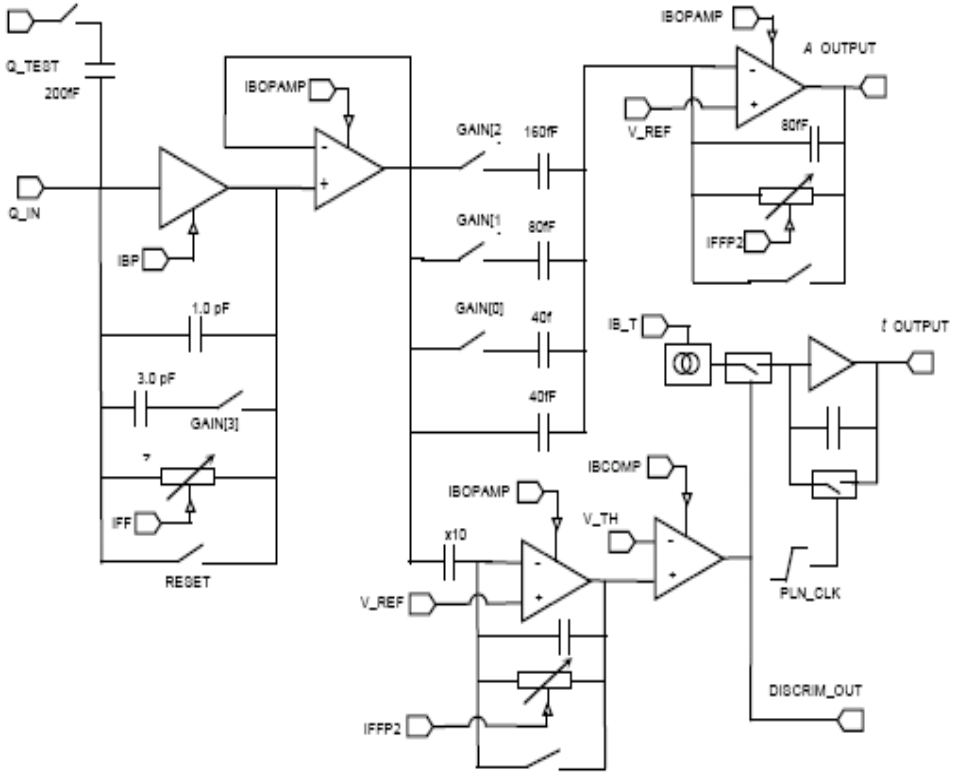


- TriP-t



TriP-t

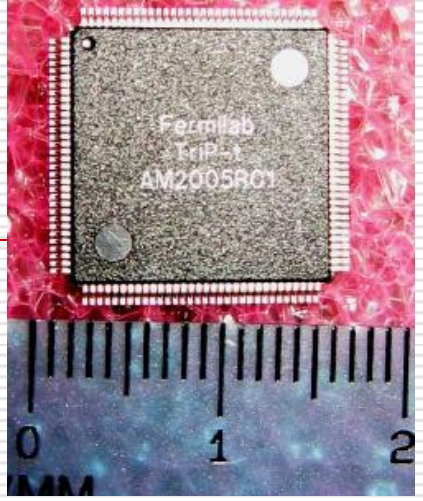
- TriP-t
  - Q sense front end :



DC stable
wide dynamic range
high bandwidth
low noise

Very flexible:
adjustible gain
adjustible bandwidth

TriP-t



- Some parameters
  - integration gate: 50ns to 20us, controlled by external clock
  - gain: 12mv/fC to 0.37mv/fC, switch set
  - pipeline depth 1 to 47, dead-timeless
  - noise: ~1fC for 40pF input capacitance
  - low power: 6.5mW/ch
  - discriminator thresh: 1/chip, 10fC to 300 fC
  - TDC: 1ns resolution

for more info: rubinov@fnal.gov

AFE and TriP-t design

TriP-t ideas:

- "keep it simple"

  do only what can not be done with commercial ICs
  ADC is external,
  zero suppression in external FPGA

- "keep it flexible"

  internal DACs (set via serial interface) can be used to adjust bandwidth, power, gain

  flexible clocking scheme, driven by FPGA

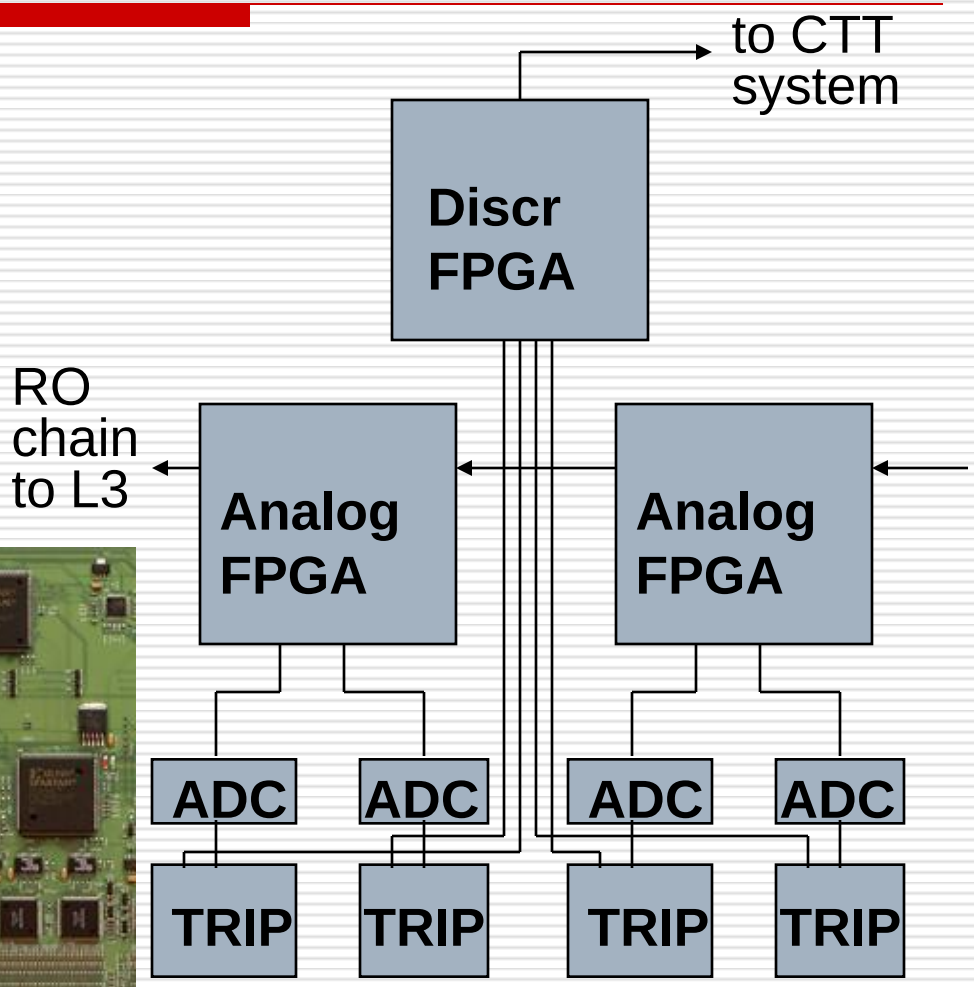
- "ease of use"

  temperature compensated to first order

  features to support testing, calibration

AFE board design

- Modular design
  - Xilinx Spartan2 FPGA to handle discr data
  - Xilinx Spartan2 FPGA to handle analog data
  - FPGAs format data
  - AFPGA used to zs and ped sub
  - Every module has its own LDOs
  - FPGAs have ident f/w- can download via slow control



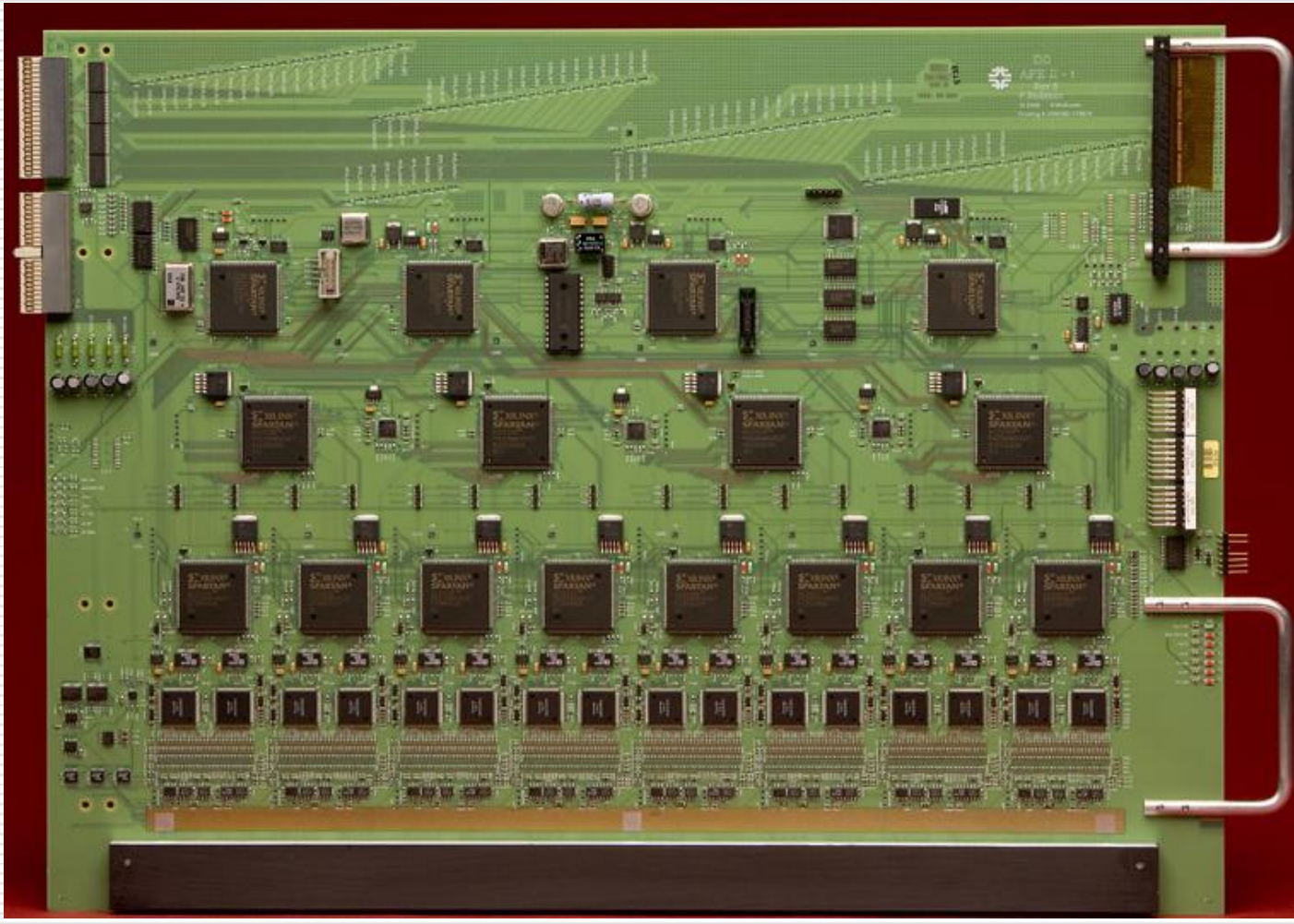
Data Flow

LVDS

4 x 1.1GPBS

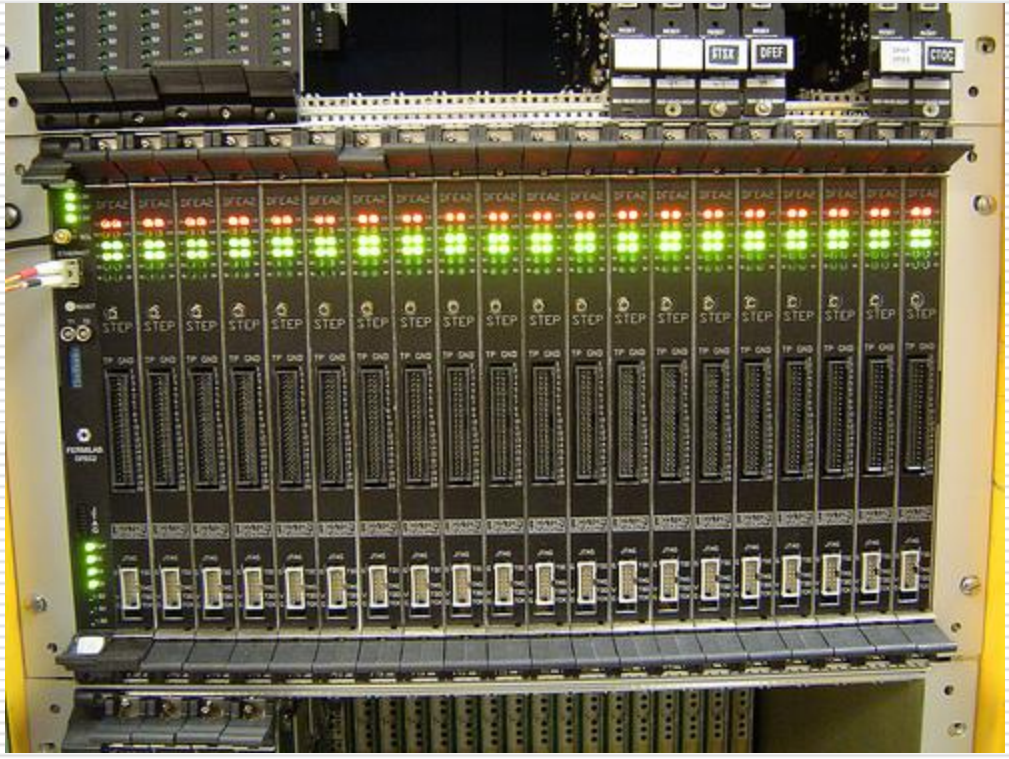
8bit @40MHZ

TTL

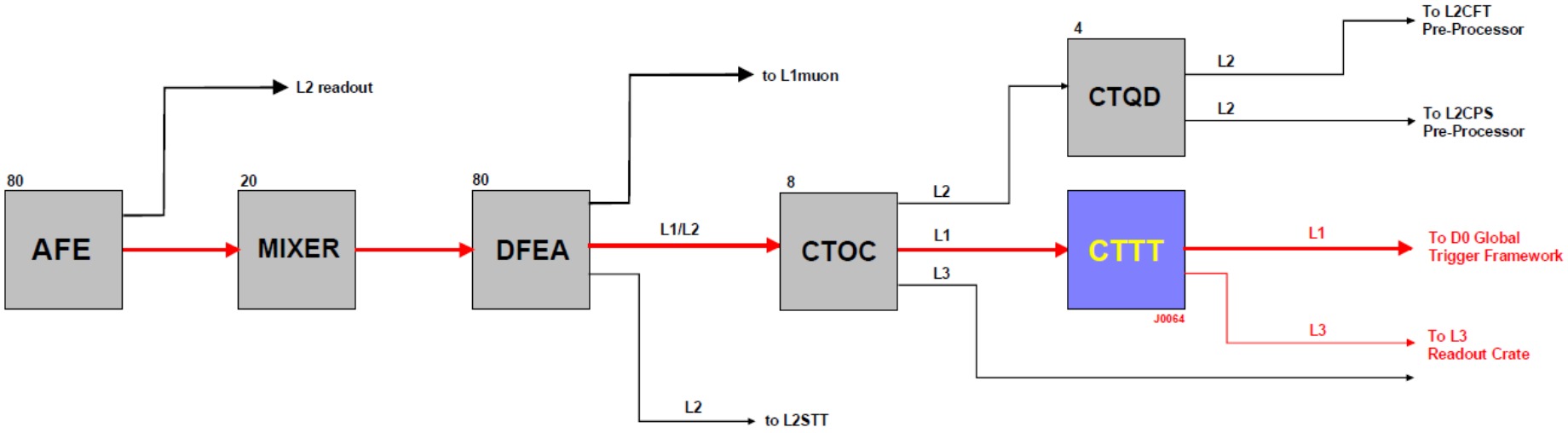


Central Track Trigger

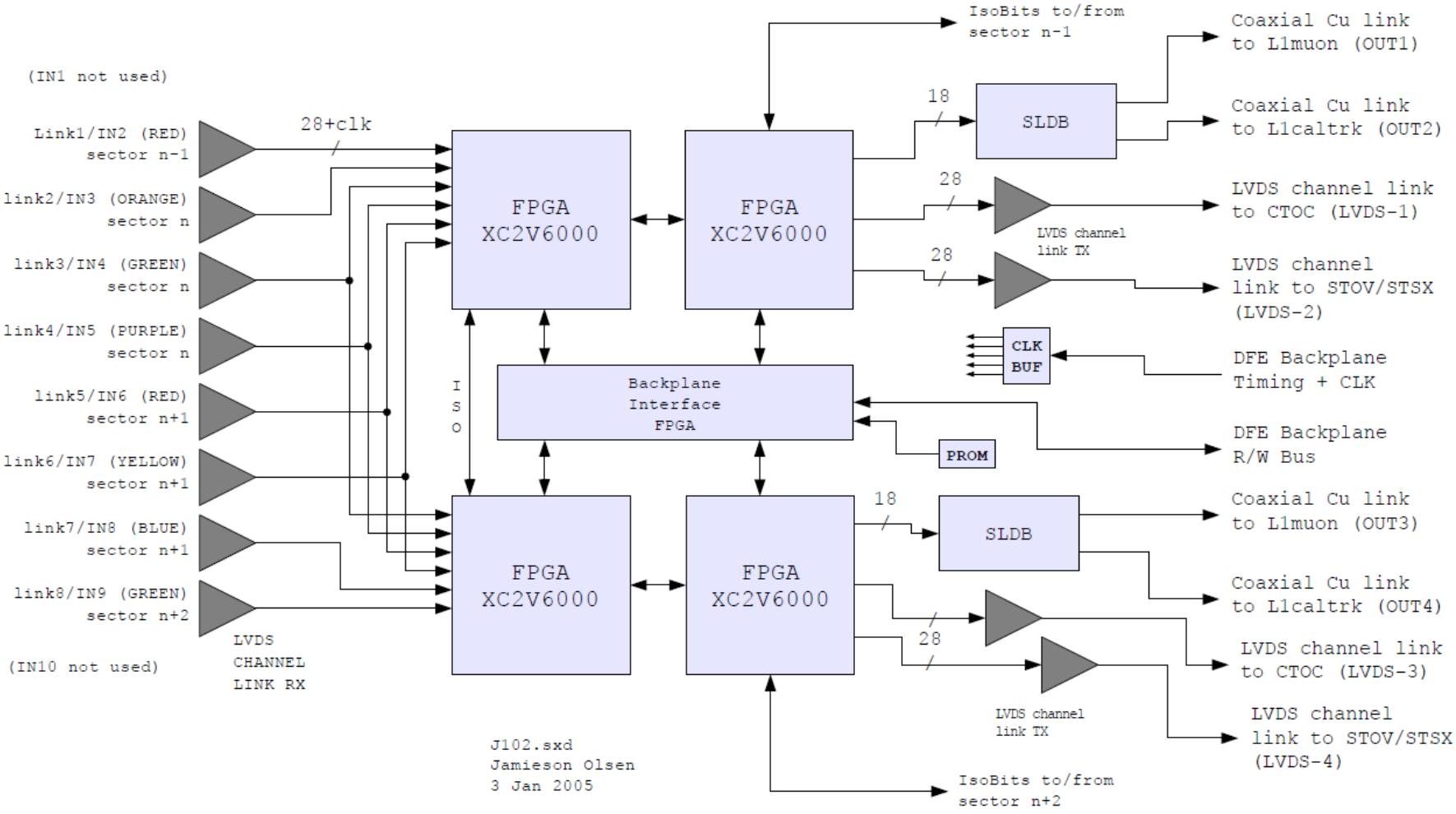
Based on DFEA2
Upgraded for RunIIb



L1CTT Chain Diagram



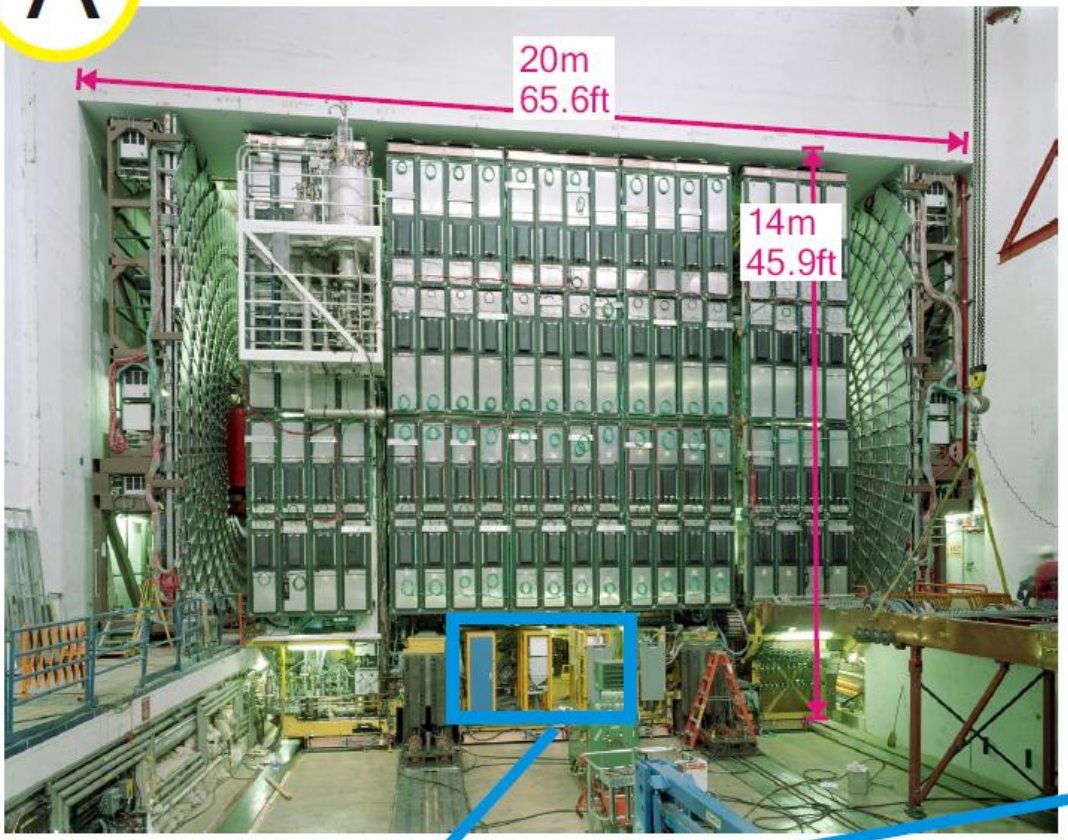
DFEA2

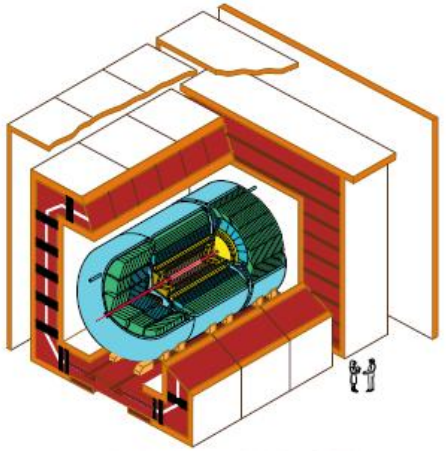

(IN1 not used)
Link1/IN2 (RED) sector n-1
link2/IN3 (ORANGE) sector n
link3/IN4 (GREEN) sector n
link4/IN5 (PURPLE) sector n
link5/IN6 (RED) sector n+1
link6/IN7 (YELLOW) sector n+1
link7/IN8 (BLUE) sector n+1
link8/IN9 (GREEN) sector n+2
(IN10 not used)
LVDS CHANNEL LINK RX
28+clk
FPGA XC2V6000
FPGA XC2V6000
FPGA XC2V6000
FPGA XC2V6000
ISO
Backplane Interface FPGA
PROM
IsoBits to/from sector n-1
IsoBits to/from sector n+2
18
SLDB
18
SLDB
28
LVDS channel link TX
28
LVDS channel link TX
28
CLK BUF
Coaxial Cu link to L1muon (OUT1)
Coaxial Cu link to L1caltrk (OUT2)
LVDS channel link to CTOC (LVDS-1)
LVDS channel link to STOV/STSX (LVDS-2)
DFE Backplane Timing + CLK
DFE Backplane R/W Bus
Coaxial Cu link to L1muon (OUT3)
Coaxial Cu link to L1caltrk (OUT4)
LVDS channel link to CTOC (LVDS-3)
LVDS channel link to STOV/STSX (LVDS-4)
J102.sxd
Jamieson Olsen
3 Jan 2005

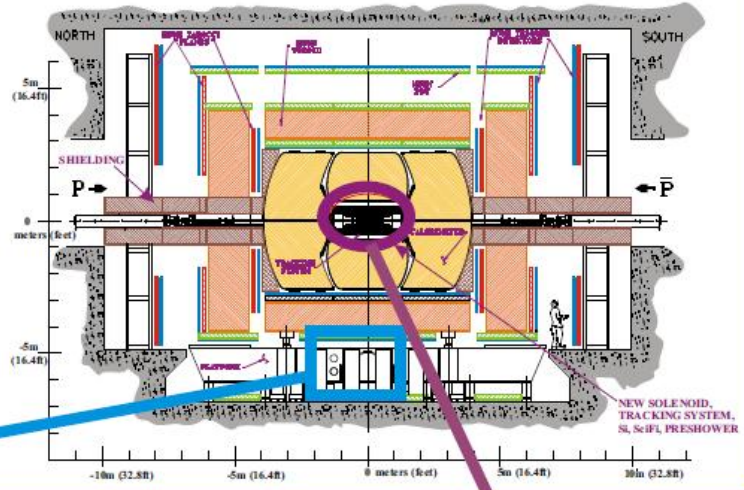
The whole picture

A

D0 Detector







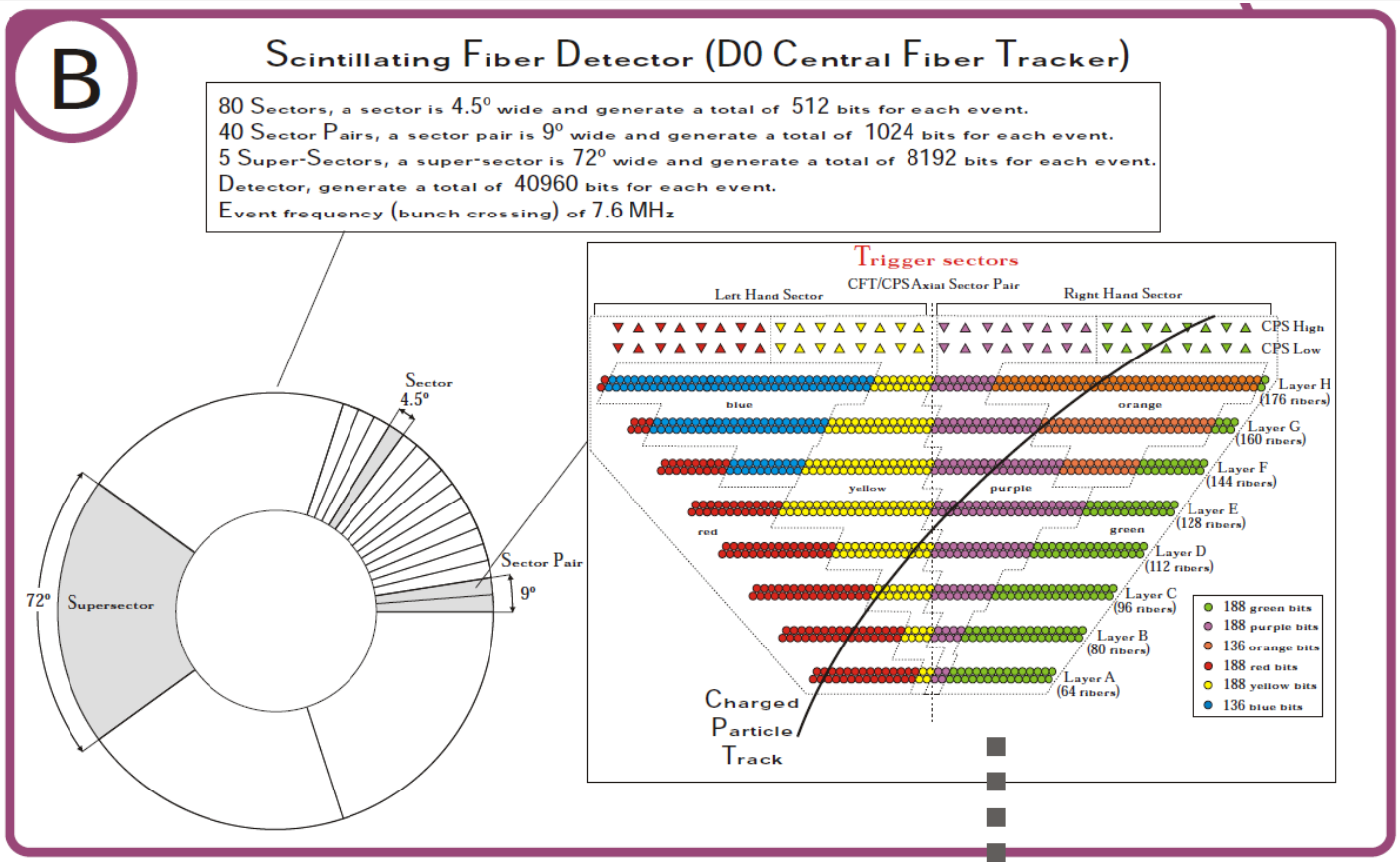
Central Fiber Tracker Electronics

Mixer

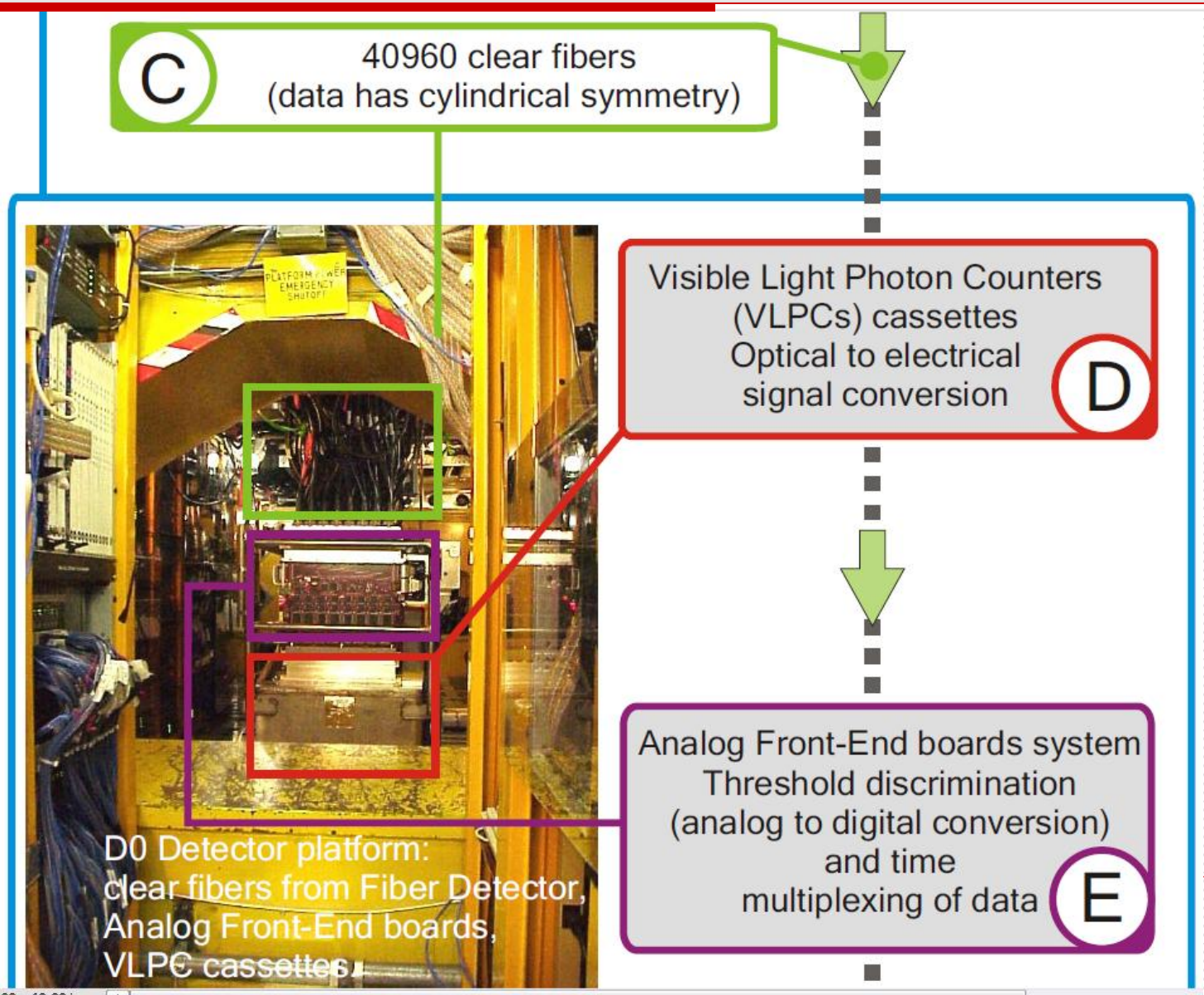
- Horrible mapping problem:

  Fiber ribbons (and AFE) are organized in cylinders

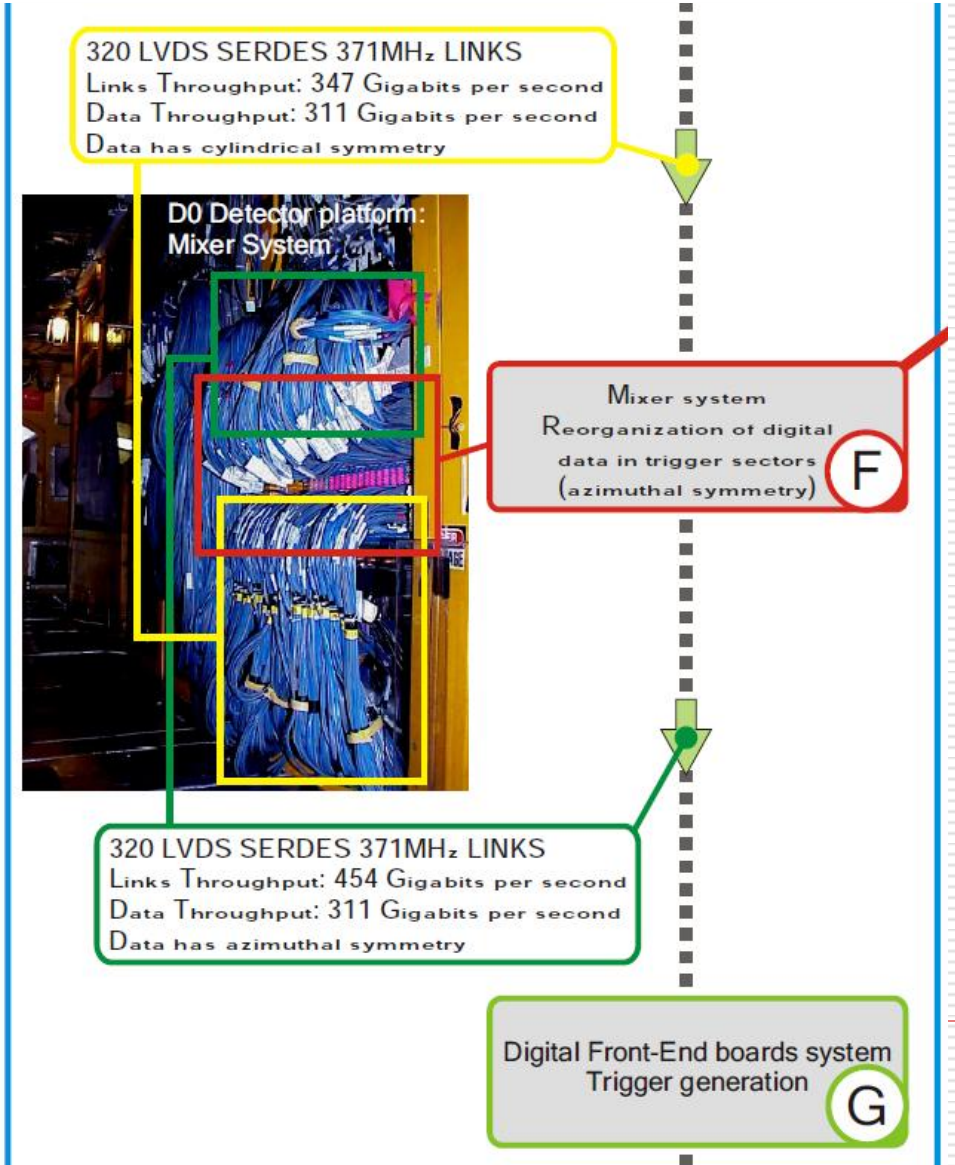
  Trigger needs to work in wedges



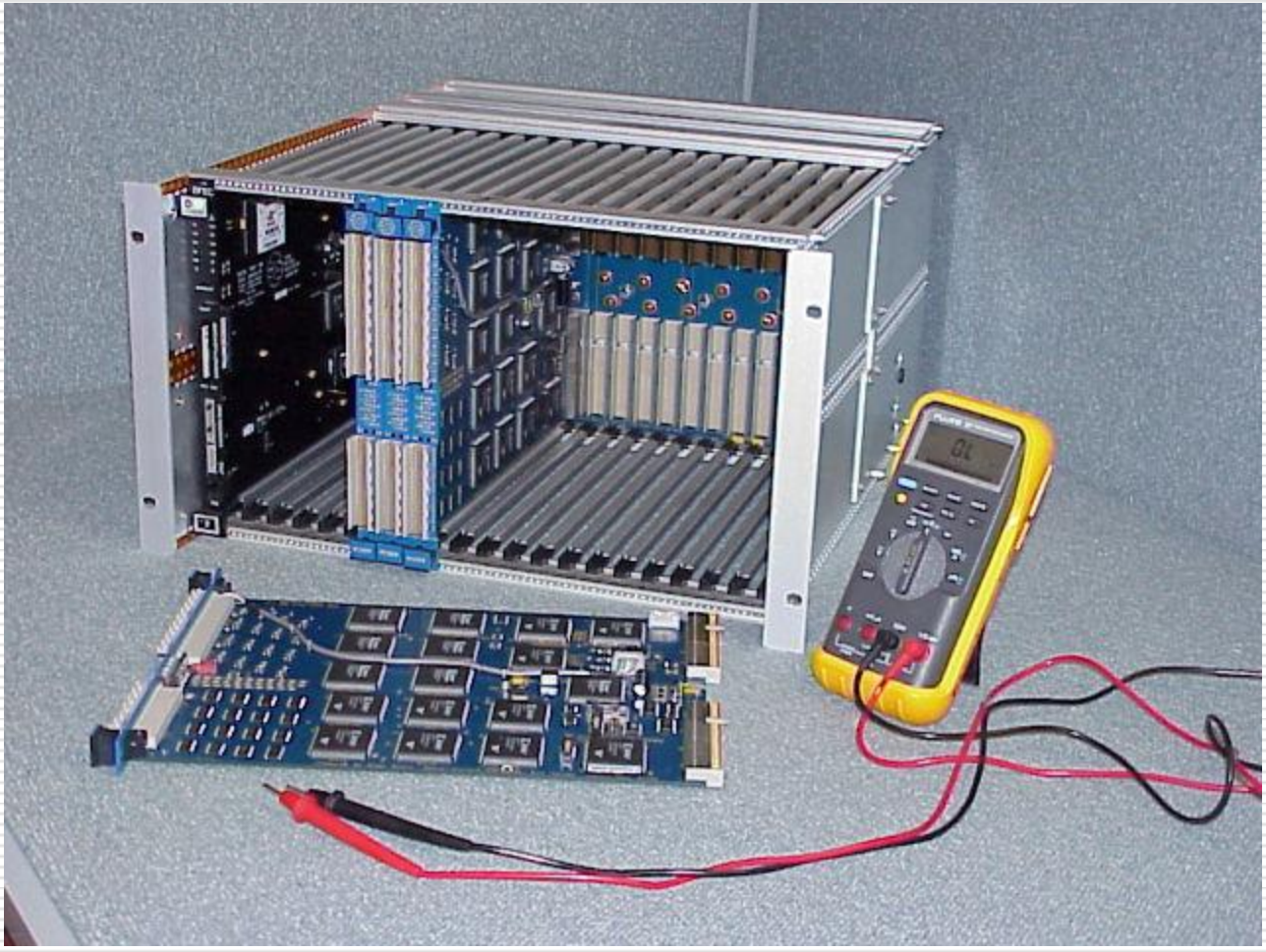
Overview (cont)



Overview (cont)



Overview (cont)

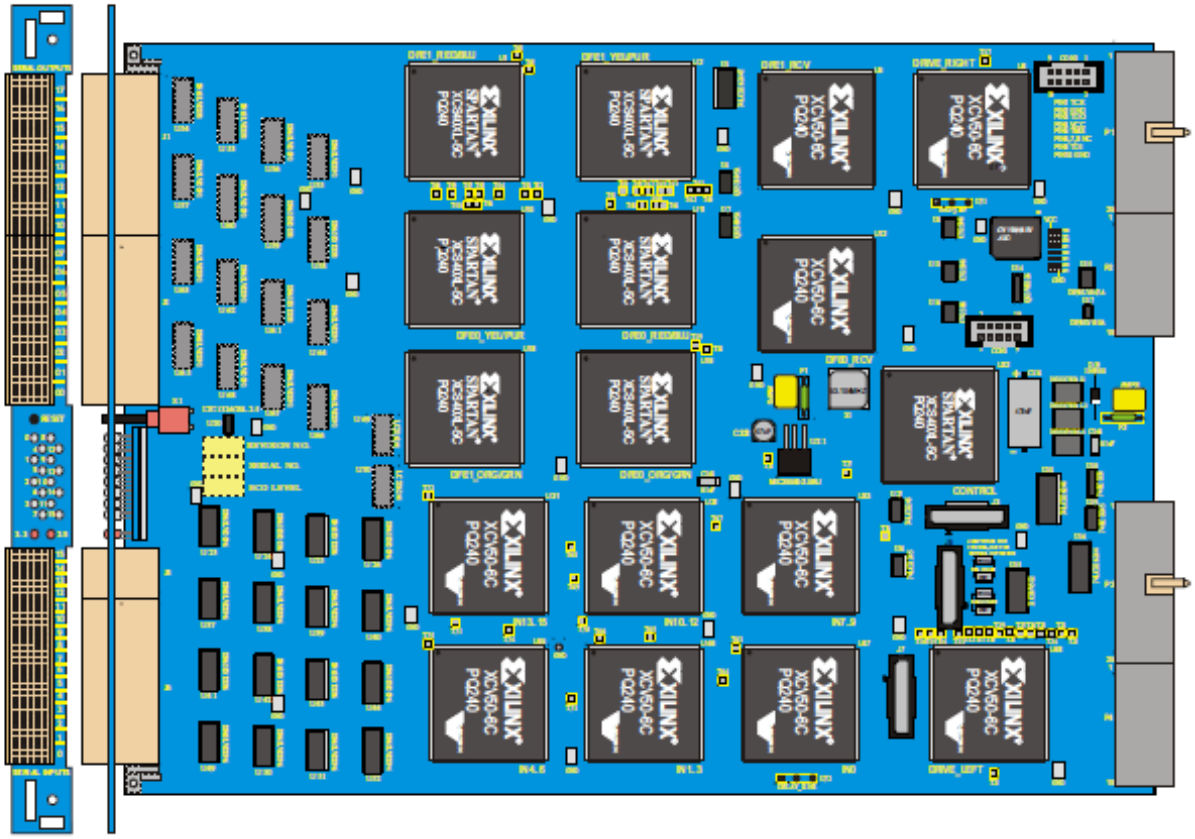


Mixer

The MIXER is a brilliant bit of engineering

But its getting a bit long in the tooth

It's the only part of the system that is not version II



Summary

- Dzero is a complex system
  - some parts are easy to repurpose
  - some parts are not
- The largest investment, BY FAR, is intellectual
  - hardware is a drop in the bucket by comparison

- You can probably reuse much of the hardware
- Don’t underestimate the re-engineering required

SPARE SLIDES AFTER THIS POINT